

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Errors
1	BRS	L1	238	gate adj oxide with thick\$4 and oxidation with resistance	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 21:38		0
2	BRS	L2	48	gate adj oxide with thick\$4 and oxidation adj resistance	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 21:39		0
3	BRS	L3	27	gate adj oxide with thick\$4 and oxidation adj resistance with film	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 21:40		0
4	BRS	L6	5	gate adj oxide with thick\$4 and oxidation adj resistance adj film and transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 21:41		0
5	BRS	L5	21	gate adj oxide with thick\$4 and oxidation adj resistance with film and transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 21:54		0
6	BRS	FAMILY	1	1980-01107C.NRA N.	DERWENT	2002/07/24 22:14		0
7	BRS	L4	18	gate adj oxide with thick\$4 and oxidation adj resistance with layer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/24 22:20		0

DERWENT-ACC-NO: 1980-01107C
DERWENT-WEEK: 198001
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TITLE: IGFET semiconductor device with irregular gate
oxide film - made by
covering part of the gate oxide film with oxidn.-resistant
material and
heat-treating

PATENT-ASSIGNEE: MATSUSHITA ELECTRONICS CORP[MATE]

PRIORITY-DATA: 1974JP-0096433 (August 20, 1974)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
PAGES	MAIN-IPC	
JP 79040353 B	December 3, 1979	N/A
000	N/A	
JP 51027074 A	March 6, 1976	N/A
000	N/A	

INT-CL (IPC): H01L029/78

ABSTRACTED-PUB-NO: JP79040353B

BASIC-ABSTRACT: For making a gate oxide film with a
different thickness on a
semiconductor substrate, a gate oxide film with uniform
thickness is deposited
on the substrate surface. A part of the gate oxide film is
covered with an
oxidn.-resistant material. Thereafter, the substrate is
heat-treated to
increase the oxide film which is not covered with the
oxidn.-resistant
material.

TITLE-TERMS:

IGFET SEMICONDUCTOR DEVICE IRREGULAR GATE OXIDE FILM MADE
COVER PART GATE OXIDE
FILM OXIDATION RESISTANCE MATERIAL HEAT TREAT

ADDL-INDEXING-TERMS:

INSULATE FIELD EFFECT TRANSISTOR

DERWENT-CLASS: L03 U12

CPI-CODES: L03-D03D; L03-D04A;

(2A) ~~***~~

See English translation before allowance

DERWENT-ACC-NO: 1996-418145
DERWENT-WEEK: 199642
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TITLE: Semiconductor device mfg method for LSI of LCD
drive - involves
selective removal of first gate oxide film and then
carrying out gate
oxidisation process again, resulting in formation of second
gate oxide film
thicker than first

PATENT-ASSIGNEE: SANYO ELECTRIC CO LTD[SAOL]

PRIORITY-DATA: 1995JP-0007705 (January 20, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
PAGES	MAIN-IPC	
JP 08204022 A	August 9, 1996	N/A
008	H01L 021/8234	

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO
APPL-DATE		
JP08204022A	N/A	1995JP-0007705
January 20, 1995		

INT-CL (IPC): H01L021/8234; H01L027/088 ; H01L029/78

ABSTRACTED-PUB-NO: JP08204022A

BASIC-ABSTRACT: The method involves forming two MOS
transistors on a substrate
(11), with the gate oxide film of one transistor thicker
than that of the
other. Initially, two SiN films (13A,13B) are formed on
the substrate. A
resist film (15) is formed covering the second SiN film. A
first ion
implantation process is carried out under which boron ions
are made to
penetrate the first SiN film and gate impregnated in the
LOCOS oxide film

formation area of the substrate, and an acceleration voltage of 40KeV. As a result, a first pouring layer (16) comes to be formed. A second ion implantation process, results in the formation of a second pouring layer (17) by pouring boron ions into the MOS transistor formation area in the substrate, under an acceleration voltage of 140KeV. For both the processes, the second SiN film, with the resist layer covering it, acts as a mask.

A LOCOS oxide film comes to be formed by a heat oxidation process, using the second SiN film as an oxidation resistance mask, after removing the resist film. A first oxidation process results in the formation of a first gate oxide film, after the removal of the second SiN film. A third ion implantation process uses the LOCOS oxide film as a mask, and impurity ions are poured into the two transistor formation areas of the substrate. The first gate oxide film is then selective removed. A second oxidation process results in the formation of a second gate oxide film, thicker than the first.

ADVANTAGE - Enables controlling limit value of each transistor to desired value. Reduces frequency of mask alignment required for ion implantation. Reduces power consumption. Contributes to rationalisation of mfg process.

CHOSEN-DRAWING: Dwg.9/20

TITLE-TERMS:

SEMICONDUCTOR DEVICE MANUFACTURE METHOD LSI LCD DRIVE
SELECT REMOVE FIRST GATE
OXIDE FILM CARRY GATE OXIDATION PROCESS RESULT FORMATION
SECOND GATE OXIDE FILM
THICK FIRST

DERWENT-CLASS: L03 U11 U13

CPI-CODES: L04-C02B; L04-C06B; L04-C12A; L04-C12B; L04-C16;
L04-E01B;

EPI-CODES: U11-C05B9; U13-D02A;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C1996-131427

Non-CPI Secondary Accession Numbers: N1996-352398